

What is Claimed is:

1 1. A parallel signal automatic phase adjusting circuit having
2 a number of data signal channels inputted together with a clock
3 signal and adjusting the clock signal so that the clock signal
4 is synchronized with each of the data signals, the parallel
5 signal automatic phase adjusting circuit comprising:

6 a signal generator for generating a signal having a
7 predetermined frequency smaller than a frequency which is
8 utilized as the data signal or the clock signal;

9 an oscillating circuit for generating a clock signal
10 having a frequency smaller than the inputted clock signal by
11 the predetermined frequency generated from the signal
12 generator; and

13 adjusting circuits provided in correspondence to the
14 respective data signal channels for effecting adjustment on
15 the clock signal generated from the oscillating circuit so that
16 the clock signal is synchronized with the corresponding data
17 signal, based on an arithmetic operation of trigonometric
18 functions using phase comparing information deriving from
19 comparison between each of the data signal and the clock signal
20 generated from the oscillating circuit and frequency
21 information regarding the respective data signals, the clock
22 signal generated from the oscillating circuit and the signal
23 supplied from the signal generator.

1 2. A parallel signal automatic phase adjusting circuit having
2 a number of data signal channels inputted together with a clock

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3 signal and adjusting the clock signal so that the clock signal
4 is synchronized with each of the data signals, the parallel
5 signal automatic phase adjusting circuit comprising:

6 an oscillating circuit for generating a clock signal
7 having a frequency smaller than the inputted clock signal by
8 a predetermined frequency; and

9 adjusting circuits provided in correspondence to the
10 respective data signal channels for effecting adjustment on
11 the clock signal generated from the oscillating circuit so that
12 the clock signal is synchronized with the corresponding data
13 signal, based on an arithmetic operation of trigonometric
14 functions using as a parameter, phase comparing information
15 deriving from comparison between each of the data signal and
16 the clock signal generated from the oscillating circuit,
17 frequency information regarding the clock signal and the data
18 signals, and the frequency information of the predetermined
19 frequency.

1 3. A parallel signal automatic phase adjusting circuit having
2 a number of data signal channels inputted together with a clock
3 signal and adjusting the clock signal so that each clock signal
4 is synchronized with each of the data signals, the parallel
5 signal automatic phase adjusting circuit comprising:

6 adjusting circuits provided in correspondence to the
7 respective data signal channels for effecting adjustment on
8 the clock signal generated from the oscillating circuit so that
9 the clock signal is synchronized with the corresponding data
10 signal: wherein

each of the adjusting circuits is arranged to include a phase comparator for comparing the clock signal and the data signal in phase, and

a trigonometric function calculating unit for effecting adjustment on the clock signal so that the clock signal is synchronized with the data signal, based on trigonometric function calculation using phase comparing information supplied from the phase comparator as a parameter.

4. A parallel signal automatic phase adjusting circuit according to Claim 1, wherein

each of the adjusting circuit is arranged to include a phase comparing delay circuit which is supplied with a signal from the signal generator, compares the corresponding data signal with the clock signal as a target of adjustment and generates phase comparing information therefrom as a result of comparison together with frequency information of a signal from the signal generator, and

a calculating circuit for effecting adjustment on the clock signal generated from the oscillating circuit so that the clock signal is synchronized with the corresponding data signal based on the trigonometric function calculation using the clock signal supplied from the oscillating circuit and the information supplied from the phase comparing delay circuit.

5. A parallel signal automatic phase adjusting circuit according to Claim 2, wherein

each of the adjusting circuit is arranged to include a

4 phase comparing oscillating circuit which oscillates at a
5 frequency identical to the predetermined frequency (decreased
6 by the oscillating circuit), compares the corresponding data
7 signal with the clock signal as a target of adjustment, and
8 generates phase difference information therefrom as the
9 frequency information, and

10 a calculating circuit for effecting adjustment on the
11 clock signal generated from the oscillating circuit so that
12 the clock signal is synchronized with the corresponding data
13 signal based on the trigonometric function calculation using
14 the clock signal supplied from the oscillating circuit and the
15 information supplied from the phase comparing delay circuit
16 as parameters.

1 6. A parallel signal automatic phase adjusting circuit
2 according to Claim 1, comprising an inter-data phase adjusting
3 circuit which is supplied with the clock signals having undergone
4 adjustment by the respective adjusting circuits together with
5 the corresponding data signal, and generates a plurality of
6 kinds of data in synchronism with the timing of the most delayed
7 clock signal

1 7. A parallel signal automatic phase adjusting circuit
2 according to Claim 2, comprising an inter-data phase adjusting
3 circuit which is supplied with the clock signals having undergone
4 adjustment by the respective adjusting circuits together with
5 the corresponding data signal, and generates a plurality of kinds
6 of data in synchronism with the timing of the most delayed clock

7 signal.

1 8. A parallel signal automatic phase adjusting circuit
2 according to Claim 3, comprising an inter-data phase adjusting
3 circuit which is supplied with the clock signals having undergone
4 adjustment by the respective adjusting circuits together with
5 the corresponding data signal, and generates a plurality of
6 kinds of data in synchronism with the timing of the most delayed
7 clock signal.

1 9. A parallel signal automatic phase adjusting circuit
2 according to Claim 6, wherein the inter-data phase adjusting
3 circuit is arranged to include a clock selecting circuit for
4 selecting a clock signal having the most delayed timing from
5 clock signals having undergone adjustment in the respective
6 adjusting circuits, and
7 a data output section for generating at the same timing
8 data signals other than the data signal corresponding to the
9 clock signal selected by the clock selecting circuit, based
10 on the clock signal selected by the clock selecting circuit.

1 10. A parallel signal automatic phase adjusting circuit
2 according to Claim 7, wherein the inter-data phase adjusting
3 circuit is arranged to include a clock selecting circuit for
4 selecting a clock signal having the most delayed timing from
5 clock signals having undergone adjustment in the respective
6 adjusting circuits, and
7 a data output section for generating at the same timing

8 data signals other than the data signal corresponding to the
9 clock signal selected by the clock selecting circuit, based on
10 the clock signal selected by the clock selecting circuit.

1 11. A parallel signal automatic phase adjusting circuit
2 according to Claim 8, wherein the inter-data phase adjusting
3 circuit is arranged to include a clock selecting circuit for
4 selecting a clock signal having the most delayed timing from
5 clock signals having undergone adjustment in the respective
6 adjusting circuits, and

7 a data output section for generating at the same timing
8 data signals other than the data signal corresponding to the
9 clock signal selected by the clock selecting circuit, based
10 on the clock signal selected by the clock selecting circuit.

1 12. A parallel signal automatic phase adjusting circuit
2 according to Claim 9, wherein the data output section is composed
3 of a number of data output units provided so as to correspond
4 to the data signal channels, respectively, each of the data
5 output units being made up of a flip-flop circuit operable in
6 response to the selected clock signal.

1 13. A parallel signal automatic phase adjusting circuit according
2 to Claim 10, wherein the data output section is composed of a
3 number of data output units provided so as to correspond to the
4 data signal channels, respectively, each of the data output units
5 being made up of a flip-flop circuit operable in response to
6 the selected clock signal.

7 corresponding to the selected clock signal,
8 a data output section for generating all of the data signals
9 at the same timing based on the clock signal selected by the
10 clock selecting circuit, and
11 a register circuit section capable of compensating for
12 a phase deviation exceeding one time slot amount based on bit
13 information of respective data signals.

17. A parallel signal automatic phase adjusting circuit
according to Claim 8, wherein the inter-data phase adjusting
circuit is arranged to include a clock selecting circuit for
selecting a clock signal having the most delayed timing from
clock signals having undergone adjustment in the respective
adjusting circuits, and for generating a data signal
corresponding to the selected clock signal,
a data output section for generating all of the data
signals at the same timing based on the clock signal selected
by the clock selecting circuit, and
a register circuit section capable of compensating for
a phase deviation exceeding one time slot amount based on bit
information of respective data signals.

18. A parallel signal automatic phase adjusting circuit
according to Claim 15, wherein the register circuit section
is arranged to include a plurality of shift registers connected
in a cascade fashion so as to correspond to respective data
signal channels, each of the shift registers being capable of
holding data of corresponding data signal channel, and

7 selectors provided so as to correspond to respective data
8 signal channels so that each selector is supplied with an output
9 signal from the shift registers in the corresponding data signal
10 channel, all of the selectors being capable of outputting
11 respective data stream at the same timing in response to a select
12 signal useful for extracting data pieces having the same timing.

1 19. A parallel signal automatic phase adjusting circuit
2 according to Claim 16, wherein the register circuit section is
3 arranged to include a plurality of shift registers connected
4 in a cascade fashion so as to correspond to respective data signal
5 channels, each of the shift registers being capable of holding
6 data of corresponding data signal channel, and

7 selectors provided so as to correspond to respective data
8 signal channels so that each selector is supplied with an output
9 signal from the shift registers in the corresponding data signal
10 channel, all of the selectors being capable of outputting
11 respective data stream at the same timing in response to a select
12 signal useful for extracting data pieces having the same timing.

1 20. A parallel signal automatic phase adjusting circuit
2 according to Claim 17, wherein the register circuit section
3 is arranged to include a plurality of shift registers connected
4 in a cascade fashion so as to correspond to respective data
5 signal channels, each of the shift registers being capable of
6 holding data of corresponding data signal channel, and

7 selectors provided so as to correspond to respective data
8 signal channels so that each selector is supplied with an output

9 signal from the shift registers in the corresponding data signal
10 channel, all of the selectors being capable of outputting
11 respective data stream at the same timing in response to a select
12 signal useful for extracting data pieces having the same timing.

1 21. A parallel signal automatic phase adjusting circuit
2 according to Claims 1, wherein each of the adjusting circuits
3 is arranged to include a temperature sensor for compensating
4 for the temperature dependability of the phase comparing
5 information.

1 22. A parallel signal automatic phase adjusting circuit
2 according to Claims 2, wherein each of the adjusting circuits
3 is arranged to include a temperature sensor for compensating
4 for the temperature dependability of the phase comparing
5 information.

1 23. A parallel signal automatic phase adjusting circuit
2 according to Claims 3, wherein each of the adjusting circuits
3 is arranged to include a temperature sensor for compensating
4 for the temperature dependability of the phase comparing
5 information.